TITLE OF THE INVENTION

# METHOD AND APPARATUS FOR POWER SUPPLY CAPABLE OF EFFECTIVELY REDUCING A POWER CONSUMPTION

## FIELD OF THE INVENTION

[0001] This patent specification relates to a method and apparatus for power supply, and more particularly to a method and apparatus for power supply that effectively reducing a power consumption.

## BACKGROUND OF THE INVENTION

[0002] Conventionally, a power supply apparatus that reduces a direct current supplied from a direct current power source (e.g., a battery) to a predetermined voltage is classified into two types; one type using a voltage regulator and the other type using a DC-to-DC converter.

[0003] Fig. 1 shows an exemplary circuit of a background power supply apparatus using a voltage regulator 100. In the voltage regulator 100 of Fig. 1, a P-channel-type MOS (metal oxide semiconductor) transistor 102 (hereinafter referred to as a P-MOS transistor 102) and resisters 103 and 104 are connected in series between a source power terminal applied with a source power voltage VDD by a direct current 101 (e.g., a battery including a secondary battery) and a grounding. The resisters 103 and 104 divide a voltage Vout which is compared by a voltage comparator 106 with a predetermined reference voltage Vref generated by a reference voltage generator 105. Based on a comparison result, an operation of the P-MOS transistor 102 is controlled so that the voltage Vout is held at a

desired value. In Fig. 1, a CPU 107 is an exemplary system that requires power from the voltage regulator 100.

[0004] However, the above-described voltage regulator has a drawback that the P-MOS transistor 101 consumes a great amount of electric power for a reduction of the source power voltage VDD to the voltage Vout. More specifically, when the CPU 107 consumes a current of 100 mA, for example, and a voltage regulator 100 reduces the source power voltage VDD from 3.6 volts, for example, to 2 volts, for example, the P-MOS transistor 101 consumes the power of 0.16 W. That is, the voltage regulator consumes a difference of the battery voltage and the CPU's operational voltage. Such voltage regulator is undesirable for a system aiming a low power consumption since the CPU's operational voltage has been lowered in the recent years.

[0005] Accordingly, as shown in Fig. 2, a DC-to-DC converter is used in place of the voltage regulator as a power supply in a system (e.g., the CPU 107) using a battery. In Fig. 2, a DC-to-DC converter 110 reduces the source power voltage VDD to a predetermined voltage Vout and supplies the voltage Vout to the CPU 107.

[0006] In general, a system using a battery as a source of power is provided with a sleep function for temporarily stopping the operations of the system to reduce an electrical power consumption on an as needed basis. In the case of the power supply apparatus of Fig. 2, it is attempted to reduce the power consumption by changing the output terminal of the DC-to-DC converter 110 to the CPU 107

in the sleep mode from a grounding level to a high impedance level. This is because the DC-to-DC converter 110 is used as an apparatus that directly controls the source power required by the system (e.g., the CPU 107).

[0007] On the other hands, the DC-to-DC converter 110 is required to be always in an active state in the case the system (e.g., the CPU 107) in the sleep mode is intermittently activated to control certain components on an as needed basis. In such a case, the power consumption by the DC-to-DC converter 110 shares a large part of the total system power consumption.

## SUMMARY OF THE INVENTION

[0008] This patent specification describes a novel power supply apparatus. In one example, this novel power supply apparatus includes a DC-to-DC converter and a voltage regulator. The DC-to-DC converter is arranged and configured to perform a voltage conversion for converting a voltage of a source power supplied from a direct current power source to a first predetermined voltage. The first predetermined voltage is lower than the voltage of the source power. The voltage regulator is arranged and configured to carrying out a voltage regulation for regulating the first predetermined voltage of the source power to at least a second predetermined voltage. The second predetermined voltage is lower than the first predetermined voltage.

[0009] The DC-to-DC converter may be turned into a non-active state to stop the voltage conversion and straight passes the voltage of the source power when an operation mode is changed to a sleep mode.

[00010] The DC-to-DC converter may include a switching circuit, a smoothing circuit, and a controller. The switching circuit is arranged and configured to perform a switching operation for switching the source power and to output a pulsating current voltage. The smoothing circuit is arranged and configured to smooth the pulsating current voltage output by the switching circuit and to output a smoothed voltage to the voltage regulator. The controller is arranged and configured to detect the smoothed voltage output from the smoothing circuit and to control the switching circuit to change a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output by the smoothing circuit is substantially equal to the first predetermined voltage. The controller is turned into a non-active state to cause the switching circuit to stop the switching operation so as to pass the voltage of the source power through the switching circuit and to output the voltage of the source power to the smoothing circuit when the operation mode is changed to the sleep mode.

[00011] The DC-to-DC converter may output the voltage of the source power without performing the voltage conversion when the operation mode is changed to the sleep mode.

[00012] The converter may include a switching circuit, a smoothing circuit, and a controller. The switching circuit is arranged and configured to perform a switching operation for switching the source power and outputting a pulsating current voltage. The smoothing circuit is arranged and configured to smooth the

pulsating current voltage output from the switching circuit and to output a smoothed voltage to the voltage regulator. The controller is arranged and configured to detect the smoothed voltage output from the smoothing circuit and to control the switching circuit to change a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output from the smoothing circuit is substantially equal to the first predetermined voltage. The controller causes the switching circuit to stop the switching operation so as to pass the voltage of the source power through the switching circuit and to output the voltage of the source power to the smoothing circuit when the operation mode is changed to the sleep mode.

[00013] The controller may connect a load to an output terminal of the smoothing circuit and controls a current flowing the load so as to reduce the voltage output from the smoothing circuit to the first predetermined voltage when the voltage output from the smoothing circuit is lower than the first predetermined voltage and when the operation mode is changed to a normal operation mode.

[00014] The controller may include a transistor, a comparator, and a current control circuit. The transistor operates as the load. The comparator performs a first comparison for comparing the voltage output from the smoothing circuit with the first predetermined voltage when the operation mode is changed to the normal operation mode and outputs a first comparison result. The current control circuit is arranged and configured to control the transistor to produce a current flowing

therethrough in response to the first comparison result of the comparator when the operation mode is changed to the normal operation mode.

[00015] The current control circuit may control the transistor to increase the current at a first predetermined pace when the voltage output from the smoothing circuit is determined as greater than the first predetermined voltage based on the first comparison result performed by the comparator.

[00016] The current control circuit may control the transistor to continue to increase the current at the first predetermined pace for a first predetermined time period when the voltage output from the smoothing circuit is determined as substantially equal to the first predetermined voltage based on the first comparison result performed by the comparator. The current control circuit may further control the transistor to produce a saturated current flowing therethrough for a second predetermined time period immediately after the first predetermined time period.

[00017] The current control circuit may control the transistor to decrease the current at a second predetermined pace for a third predetermined time period immediately after the second predetermined time period.

[00018] The controller may detect a current output from the switching circuit and controls the switching circuit to vary the current in response to the detected current when the operation mode is changed to the sleep mode.

[00019] The controller may control the switching circuit to straight output the voltage of the source power to the smoothing circuit when the current detected is

smaller than a predetermined value and to reduce the current output therefrom to a value smaller than the predetermined value in a predetermined manner when the current is greater than the predetermined value.

[00020] The controller may perform a second comparison between a reference voltage dropping at a substantially constant pace and the voltage output from the smoothing circuit in response to the detected voltage when the operation mode is changed to the normal operation mode, and controls a duty cycle of the switching operation performed by the switching circuit according to a result of the second comparison during a time the voltage output from the smoothing circuit is reduced to the first predetermined voltage.

[00021] The controller may perform a third comparison between another predetermined reference voltage and the voltage output from the smoothing circuit in response to the detected voltage, and controls a duty cycle of the switching operation performed by the switching circuit according to a result of the third comparison when the voltage output from the smoothing circuit is reduced to the first predetermined voltage.

[00022] This patent specification further describes a novel method of power supply. In one example, this novel method includes the steps of performing and regulating. The performing step performs a DC-to-DC conversion with a DC-to-DC converter to achieve a voltage conversion for converting a voltage of a source power supplied from a direct current power source to a first predetermined voltage. The first predetermined voltage is lower than the voltage of the source

power. The regulating step regulates the first predetermined voltage of the source power to at least a second predetermined voltage. The second predetermined voltage is lower than the first predetermined voltage.

[00023] The performing step may turn the DC-to-DC converter into a non-active state to stop the DC-to-DC conversion and straight passes the voltage of the source power through the DC-to-DC converter to the voltage regulator when an operation mode is changed to a sleep mode.

[00024] The performing step may include the steps of executing, smoothing, detecting, changing, and stopping. The executing step executes a switching operation for switching the source power to output a pulsating current voltage. The smoothing step smoothes the pulsating current voltage output by the switching circuit to output a smoothed voltage to the voltage regulator. The detecting step detects the smoothed voltage output in the smoothing step. The changing step changes a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output in the smoothing step is substantially equal to the first predetermined voltage. The stopping step stops the switching operation when the operation mode is changed to the sleep mode so as to apply the voltage of the source power to the smoothing circuit.

[00025] The DC-to-DC converter may output the voltage of the source power without performing the voltage conversion when the operation mode is changed to the sleep mode.

[00026] The performing step may include the steps of executing, smoothing, detecting, changing, and stopping. The executing step executes a switching operation for switching the source power to output a pulsating current voltage. The smoothing step smoothes the pulsating current voltage output in the switching step to output a smoothed voltage to the voltage regulator. The detecting step detects the smoothed voltage output in the smoothing step. The changing step changes a performance of the switching operation in response to a detection result of the smoothed voltage so that the smoothed voltage output in the smoothing step is substantially equal to the first predetermined voltage. The stopping step stops the switching operation when the operation mode is changed to the sleep mode so as to apply the voltage of the source power to the smoothing circuit.

[00027] The above-mentioned novel method may further includes steps of providing, applying, and adjusting. The providing step provides a transistor as a load. The applying step applies the voltage output in the smoothing step to the transistor so that a current flows through the transistor when the voltage output in the smoothing step is lower than the first predetermined voltage and when the operation mode is changed to a normal operation mode. The adjusting step adjusts the current flowing the load so as to reduce the voltage output in the smoothing step to the first predetermined voltage.

[00028] The adjusting step may include the steps of performing and causing. The performing step performs a first comparison for comparing the voltage output

in the smoothing step with the first predetermined voltage when the operation mode is changed to the normal operation mode to output a first comparison result. The causing step causes the transistor to produce a current flowing therethrough in response to the first comparison result of the comparing step when the operation mode is changed to the normal operation mode.

[00029] The causing step may cause the transistor to increase the current at a first predetermined pace when the voltage output in the smoothing step is determined as greater than the first predetermined voltage based on the first comparison result performed in the comparing step.

[00030] The causing step may cause the transistor to continue to increase the current at the first predetermined pace for a first predetermined time period when the voltage output in the smoothing step is determined as substantially equal to the first predetermined voltage based on the first comparison result performed in the comparing step, and may cause the transistor to produce a saturated current flowing therethrough for a second predetermined time period immediately after the first predetermined time period.

[00031] The causing step may cause the transistor to decrease the current at a second predetermined pace for a third predetermined time period immediately after the second predetermined time period.

[00032] The above-mentioned method may further include the steps of detecting and instructing. The detecting step detect a current output in the switching step when the operation mode is changed to the sleep mode. The

instructing step instruct the switching step to change the current in response to the detected current.

[00033] The instructing step may instruct the switching step to straight output the voltage of the source power to the smoothing step when the current detected is smaller than a predetermined value and to reduce the current output in the switching step to a value smaller than the predetermined value in a predetermined manner when the current is greater than the predetermined value.

[00034] The novel method may further include the steps of performing and determining. The performing step performs a second comparison between a reference voltage dropping at a substantially constant pace and the voltage output in the smoothing step in response to the detected voltage during a time the voltage output in the smoothing step is reduced to the first predetermined voltage. The determining step determines a duty cycle of the switching operation performed in the switching step according to a result of the second comparison.

[00035] The above-mentioned novel method may further include the steps of performing and controlling. The performing step performs a third comparison between another predetermined reference voltage and the voltage output in the smoothing circuit in response to the detected voltage. The controlling step controls the duty cycle of the switching operation performed in the switching step according to a result of the third comparison when the voltage output in the smoothing step is reduced to the first predetermined voltage.

## BRIEF DESCRIPTION OF THE DRAWINGS

[00036] A more complete appreciation of the disclosure and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

[00037] Fig. 1 is a block diagram of a background power supply apparatus;

[00038] Fig. 2 is a block diagram of another background power supply apparatus;

[00039] Fig. 3 is a block diagram of a power supply apparatus including a DC-to-DC converter according to a preferred embodiment;

[00040] Fig. 4 is a circuit diagram of the DC-to-DC converter;

[00041] Fig. 5 is a circuit diagram of another DC-to-DC converter according to a preferred embodiment;

[00042] Fig. 6 is a time chart for explaining control signals of a controller included in the DC-to-DC converter of Fig. 5;

[00043] Fig. 7 is a circuit diagram of another DC-to-DC converter according to a preferred embodiment;

[00044] Fig. 8 is a time chart for explaining an undershoot and an overshoot of an output voltage Vo;

[00045] Fig. 9 is a time chart for showing an example of a current ia flowing through an N-MOS transistor of an undershooting preventive circuit included in the DC-to-DC converter of Fig. 7;

[00046] Fig. 10 is a time chart for showing an example of a gate voltage Vg relative to the N-MOS transistor of the undershooting preventive circuit;

[00047] Fig. 11 is a time chart for showing another example of the gate voltage Vg relative to the N-MOS transistor of the undershooting preventive circuit;

[00048] Fig. 12 is a time chart for showing an example of the output voltage Vo output by the DC-to-DC converter of Fig. 7;

[00049] Fig. 13 is a time chart for explaining a relationship among the voltage Vo, a divided voltage Vd, and a reference voltage Vr1 generated in the DC-to-DC converter of Fig. 7;

[00050] Fig. 14 is a circuit diagram of another DC-to-DC converter according to a preferred embodiment; and

[00051] Fig. 15 is a time chart for explaining a relationship among a voltage Vo, a divided voltage Vd, and a reference voltage Vr1 generated in the DC-to-DC converter of Fig. 14.

## DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[00052] In describing preferred embodiments illustrated in the drawings, specific terminology is employed for the sake of clarity. However, the disclosure of this patent specification is not intended to be limited to the specific terminology so selected and it is to be understood that each specific element includes all technical equivalents that operate in a similar manner.

[00053] Referring now to the drawings, wherein like reference numerals designate identical or corresponding parts throughout the several views, and more particularly to Fig. 3 thereof, a power supply apparatus 1 according to a preferred embodiment is described. As illustrated in Fig. 3, the power supply apparatus 1 includes a DC-to-DC (direct current to direct current) converter 2, and a voltage regulator 3. The DC-to-DC converter 2 reduces a power source voltage VDD to a predetermined voltage Va and has an output terminal outputting the voltage Va. The power source voltage VDD is supplied from a direct current power source 10 that can be composed of various kinds of batteries including secondary batteries. The voltage regulator 3 reduces the predetermined voltage Va output from the DC-to-DC converter 2 to a predetermined voltage Vb and has an output terminal outputting the voltage Vb.

[00054] As shown in Fig. 3, in the power supply apparatus 1, the DC-to-DC converter 2 is connected between the power supply line from the current power source 10 and the grounding. The voltage regulator 3 is connected between the output terminal of the DC-to-DC converter 2 and the grounding. The output terminal of the voltage regulator 3 is connected to a power supply terminal of a CPU (central processing unit) 11. The CPU 11 is shown as an exemplary device requiring a power supply. Other devices such as a DSP (digital signal processor), memories, and so on which form, together with the CPU 11, a system apparatus also require a power supply.

[00055] The voltage regulator 3 includes a P-channel-type MOS (metal oxide semiconductor) transistor 21 (hereinafter referred to as a P-MOS transistor 21), resisters 22 and 23, a reference voltage generator 24, and a voltage comparator 25. The P-MOS transistor 21 and the resisters 22 and 23 are connected in series between the output terminal of the DC-to-DC converter 2 and the grounding, and the voltage regulator 3 has an output terminal drawn from a line connecting the P-MOS transistor 21 to the resister 22. The voltage comparator 25 has an input terminal connected to a line placed between the resisters 22 and 23 and another input terminal to receive a reference voltage Vref output from the reference voltage generator 24. The voltage comparator 25 has an output terminal connected to a gate of the P-MOS transistor 21.

[00056] The resisters 22 and 23 divide the voltage Vb, and the voltage comparator 25 compares the voltage divided by the resisters 22 and 23 to the reference voltage Vref output from the reference voltage generator 24. When the divided voltage is equal to or greater than the reference voltage Vref, the voltage comparator 25 controls the operation of the P-MOS transistor 21 so that a current flowing the P-MOS transistor 21 is reduced. On the other hands, when the divided voltage is smaller than the reference voltage Vref, the voltage comparator 25 controls the P-MOS transistor 21 to increase the flowing current.

[00057] The CPU 11 has a sleep function for turning the connected system apparatus into a low power consuming state (hereinafter referred to as a sleep mode) by temporarily stopping operations of the associated components. To turn

into the sleep mode, the CPU 11 sends a sleep signal SLP to the DC-to-DC converter 2. In a normal operation mode, that is, not in the sleep mode, no sleep signal SLP is sent to the DC-to-DC converter 2 from the CPU 11 and the DC-to-DC converter 2 generates the voltage Va by reducing the power source voltage VDD supplied by the direct current power source 10 and outputs the voltage Va to the voltage regulator 3.

[00058] The voltage regulator 3 reduces the voltage Va applied as a source power by the DC-to-DC converter 2 to obtain the voltage Vb and supplies the voltage Vb to the CPU 11 as a source power. In this way, the power supply apparatus 1 reduces the power source voltage VDD supplied by the direct current power source 10 to the voltage Va with the DC-to-DC converter 2, further reduces the voltage Va to the voltage Vb with the voltage regulator 3, and supplies the voltage Vb as a source power to the CPU 11. With this configuration, it is possible to minimize a value of voltage that the voltage regulator 3 bears to reduce as a load. When the power source voltage VDD is 3.6 volts, for example, the voltage Va output by the DC-to-DC converter 2 may be set to 2.0 volts, for example, and the voltage Vb output by the voltage regulator 3 may be set to 1.8 volts, for example. Thus, the power consumption of the voltage regulator 3 can be reduced.

[00059] In the sleep mode, that is, during the time the DC-to-DC converter 2 receives the sleep signal SLP from the CPU 11, the DC-to-DC converter 2 is fell into an inactive status to stop its operation. When stopping the operation, the DC-to-DC converter 2 outputs the power source voltage VDD supplied by the

direct current power source 10 straight as the voltage Va without performing the voltage reduction. Accordingly, the power source voltage VDD is applied as a source power to the voltage regulator 3. At this time, however, the CPU 11 operates in the sleep mode and consumes almost no electric power. Therefore, the voltage regulator 3 consumes almost no electric power.

[00060] On the other hands, the CPU 11 may perform its operation at intervals of a relatively short time period (e.g., 1 second) during the sleep mode. In such an operation mode at intervals, the voltage regulator 3 reduces the power source voltage VDD applied thereto through the DC-to-DC converter 2 to the voltage Vb, thereby obtaining a source power required for the CPU 11 to operate. At this time, the electric power consumed by the CPU 11 is relatively small and therefore the P-MOS transistor 21 of the voltage regulator 3 consumes a relatively small amount of electric power.

[00061] Fig. 4 illustrates an exemplary internal structure of the DC-to-DC converter 2. As illustrated in Fig. 4, the DC-to-DC converter 2 includes a switching circuit 31, a smoothing circuit 32, and a controller 33. The switching circuit 31 switches the power source voltage VDD supplied by the direct current power source 10 and outputs a resultant pulsating current voltage. The smoothing circuit 32 smoothes the pulsating current voltage output by the switching circuit 31. The controller 33 controls the switching operation of the switching circuit 31.

[00062] The switching circuit 31 includes a P-MOS transistor 41 and a parasite diode connected between a drain and a source of the P-MOS transistor 41. In the

P-MOS transistor 41, the source is applied with the power source voltage VDD from the direct current power source 10, a gate is connected to the controller 33, and the drain is connected to the smoothing circuit 32. A substrate gate of the P-MOS transistor 41 is connected to the source thereof.

[00063] The smoothing circuit 32 includes a smoothing choke coil 45, a smoothing capacitor 46, and a flywheel diode 47. The smoothing choke coil 45 and the smoothing capacitor 46 form a choke input type smoothing circuit that smoothes the pulsating current voltage input from the P-MOS transistor 41 and outputs a resultant voltage. The flywheel diode 47 has a cathode connected to an input terminal of the smoothing choke coil 45 and an anode connected to the grounding.

[00064] The direct current smoothed through the smoothing circuit 32 is output to the voltage regulator 3 as the voltage Va, as well as to the controller 33. The controller 33 outputs a pulse signal having a predetermined frequency (e.g., in a range from several hundreds kHz to one MHz) to the gate of the P-MOS transistor 41 when receiving no input of the predetermined sleep signal SLP from the CPU 11).

[00065] The controller 33 observes the voltage output from the smoothing circuit 32 and controls a duty cycle of the pulse signal output to the gate of the P-MOS transistor 41 so that the voltage output from the smoothing circuit 32 is equal to the predetermined voltage Va (e.g., 2.0 volts). More specifically, the controller 33 reduces the duty cycle so that the P-MOS transistor 41 turns on for a

relatively longer time period when the voltage output from the smoothing circuit 32 is smaller than the predetermined voltage Va. Also, the controller 33 increases the duty cycle so that the P-MOS transistor 41 turns on for a relatively shorter time period when the voltage output from the smoothing circuit 32 is greater than the predetermined voltage Va. Further, the controller 33 maintains the duty cycle when the voltage output from the smoothing circuit 32 is equal to the predetermined voltage Va.

[00066] On the other hands, the controller 33 is turned into a non-active state and stops its operation when receiving the predetermined sleep signal SLP from the CPU 11, and an input to the gate of the P-MOS transistor 41 is at a low level. Thereby, the P-MOS transistor 41 is turned into an on state, and the voltage output from the smoothing circuit 32 is equal to the power source voltage VDD supplied by the direct current power source 10.

[00067] The above-described power supply apparatus 1 has the voltage regulator 3 configured to output a single voltage Vb. Alternatively, the above-described power supply apparatus 1 may have the voltage regulator 3 outputting a plurality of different voltages. Also, the switching circuit 31 and the controller 33 of the DC-to-DC converter 2 and the voltage regulator 3 can be integrated into a single IC chip.

[00068] Fig. 5 shows a DC-to-DC converter 202 which can be used as an alternative to the DC-to-DC converter 2. The DC-to-DC converter 202 of Fig. 5 is similar to the DC-to-DC converter 2 of Fig. 4, except for a smoothing circuit

232 and a controller 233. The smoothing circuit 232 includes a high active N-channel-type MOS (metal oxide semiconductor) transistor 51 (hereinafter referred to as a N-MOS transistor 51) in place of the flywheel diode 47 of the smoothing circuit 32. The controller 233 of Fig. 5 is similar to the controller 33 of Fig. 4, except for generation of control signals S1 and S2. In the DC-to-DC converter 202, the N-MOS transistor 51 is connected between the drain of the P-MOS transistor 41 and the grounding, as shown in Fig. 5, so that the P-MOS transistor 41 and the N-MOS transistor 51 are controlled by the controller 233 with the control signals S1 and S2.

[00069] A time chart of Fig. 6 shows a relationship between the control signals S2 and S2. A shown in Fig. 6, the sleep signal SLP output by the CPU 11 is held at a low level during the normal operation mode and at a high level during the sleep mode. During the normal operation mode, the controller 233 generates the control signals S1 and S2 which differently rise and fall from each other and sends them to the P-MOS transistor 41 and the N-MOS transistor 51, respectively. Thereby, the P-MOS transistor 41 and the N-MOS transistor 51 are controlled so as not to be turned on at the same time. This N-MOS transistor 51 can be integrated with the switching circuit 31, the controller 233, and the voltage regulator 3 into a single IC chip.

[00070] In this way, the power supply apparatus 1 generates and supplies the stable predetermined voltage Vb to the CPU 11 during the time the CPU 11 operates in the normal operation mode by efficiently reducing the power source

voltage VDD to the voltage Va with the DC-to-DC converter 202 and finally regulating the voltage Va with the voltage regulator 3 to obtain the voltage Vb. Thereby, the power supply apparatus 1 can achieve a relatively low power consumption of the voltage regulator 3 in the normal operation mode. Also, during the sleep mode, the power supply apparatus 1 causes the DC-to-DC converter 202 to turn into an inactive state to reduce the power consumption, and generates the predetermined stable Vb by reducing the power source voltage VDD to the voltage Vb directly with the voltage regulator 3. That is, since the devices including the CPU, the DSP, the memories, etc. are turned into the sleep mode and do not need the power source, the voltage Vb is not used by the devices and no power is consumed. When the CPU 11, for example, operates at intervals of a predetermined time period (e.g., one second) in the sleep mode, the CPU 11 can operate with the stable voltage Vb supplied.

[00071] Fig. 7 shows a DC-to-DC converter 302 according to another preferred embodiment. The DC-to-DC converter 302 can be used as an alternative to the DC-to-DC converter 2 of Fig. 4 and is similar to it, except for a control circuit 333. This control circuit 333 can be used in place of the control circuit 233 of the DC-to-DC converter 202, as a further alternative.

[00072] As shown in Fig. 7, the control circuit 333 includes a duty control circuit 61, an undershoot preventive circuit 62, and an overshoot preventive circuit 63. The duty control circuit 61 controls a duty cycle of a pulse signal output to the gate of the P-MOS transistor 41 so that a voltage Vo output from the

smoothing circuit 32 becomes the predetermined voltage Va. The undershoot preventive circuit 62 and the overshoot preventive circuit 63 operate to protect occurrences of an undershoot and an overshoot, respectively, of the voltage Vo. Connections of the sleep signal SLP to the duty control circuit 61, the undershoot preventive circuit 62, and the overshoot preventive circuit 63 are not shown in Fig. 7, for the sake of simplicity.

[00073] Referring to Fig. 8, mechanisms causing undershooting and overshooting waveforms are explained. In the sleep mode, the input to the gate of the P-MOS transistor 41 is at a low level and the power source voltage VDD passes through the switching circuit 31 and the smoothing circuit 32 so that the voltage Vo has the same voltage level as the power source voltage VDD, as described above. When the sleep mode (referred to as M1 in Fig. 8) is changed to the normal operation mode (referred to as M2 in Fig. 8), the voltage regulator 3 needs a certain time period as a transition time (referred to as M3 in Fig. 8) to respond to the mode change. Accordingly, during the transition time the voltage Vo is maintained at a voltage level around the power source voltage VDD, which is greater than the predetermined voltage Va, for the above-mentioned certain time after the sleep mode is terminated. This causes the controller 333 to rise the voltage to a high level input to the gate of the P-MOS transistor 41 so that the P-MOS transistor 41 is turned off and shuts off the power source voltage VDD.

[00074] That is, at the end of the transition time, the voltage regulator 3 starts its operation under the condition that the voltage Vo is maintained at a voltage

level around the power source voltage VDD. This causes the DC-to-DC converter 302 to fall to a state of being loaded by the voltage regulator 3. In this case, when a load current io (e.g., 200 mA) flows from the smoothing circuit 32, the voltage Vo may be dropped so rapidly as to produce an undershooting waveform W1, as shown in Fig. 8. As a result, the voltage Vo is momentarily reduced to a value considerably smaller than the predetermined voltage Va.

[00075] On the other hands, the voltage Vo may be risen so rapidly as to produce an overshooting waveform W2, as shown in Fig. 8, when the P-MOS transistor 41 is turned on immediately after the mode is changed from the normal operation mode to the sleep mode in order to cause the power source voltage VDD to pass through the P-MOS transistor 41. In this case, the voltage Vo may produce an overshooting waveform W2, as shown in Fig. 8 and is momentarily risen over a value considerably greater than the power source voltage VDD.

[00076] The undershoot preventive circuit 62 prevents an occurrence of the above-described undershooting waveform W1 and the overshoot preventive circuit 63 prevents an occurrence of the above-described overshooting waveform W2.

[00077] The duty control circuit 61 includes a voltage detection circuit 71 and a duty controller 72. The voltage detection circuit 71 detects the voltage Vo, and the duty controller 72 controls a duty cycle of a pulse signal input to the gate of the P-MOS transistor 41 in response to the voltage Vo detected by the voltage detection circuit 71. The voltage detection circuit 71 includes an operational amplifier 73, a voltage dividing circuit 74, a Vr1 generator 75. The voltage

dividing circuit 74 divides the voltage Vo, and includes resisters 76 and 77 and an N-channel-type MOS (metal oxide semiconductor) transistor 78 (hereinafter referred to as an N-MOS transistor 78). The Vr1 generator 75 generates a reference voltage Vr1. The resisters 76 and 77 are connected in series between the line of the voltage Vo and the grounding. The N-MOS transistor 78 has a gate that receives an inverse sleep signal SLPB (not shown) generated by the inverse of the sleep signal SLP.

[00078] In the voltage detection circuit 71, the sleep signal SLP is in a low state in the sleep mode and therefore the inverse sleep signal SLPB input to the gate of the N-MOS transistor 78 is in a high state. Thereby, the N-MOS transistor 78 is turned on and is brought into conduction. The voltage Vo is then divided by the resisters 76 and 77 and a divided voltage Vd is generated between the resisters 76 and 77. The operational amplifier 73 has an inverse input terminal receiving the divided voltage Vd and a non-inverse input terminal receiving the reference voltage Vr1 output from the Vr1 generator 75. The operational amplifier 73 compares the divided voltage Vd to the reference voltage Vr1 and outputs a voltage to the duty controller 72 in response to the comparison result. The duty controller 72 generates a pulse signal having a duty cycle in response to the voltage received from the operational amplifier 73 and outputs the pulse signal to the gate of the P-MOS transistor 41.

[00079] On the other hands, when the mode is changed from the normal operation mode to the sleep mode, the sleep signal SLP in a high state is output

from the CPU 11. Accordingly, the operational amplifier 73, the Vr1 generator 75, and the duty controller 72 are caused to stop the respective operations. At the same time, in the voltage dividing circuit 74, the gate of the N-MOS transistor 78 is turned off and is out of conduction. As a result, the voltage Vo is divided and the divided voltage Vd is generated. When the duty controller 72 stops its operation, the output terminal thereof is in an open state and in a high impedance state.

[00080] The undershoot preventive circuit 62 includes an N-channel-type MOS (metal oxide semiconductor) transistor 81 (hereinafter referred to as an N-MOS transistor 81), an operations amplifier 83, and a current control circuit 83. The N-MOS transistor 81 operates as a load to consume a current ia flowing from the output terminal of the smoothing circuit 32 to the grounding. The operational amplifier 82 operates as a voltage comparator for comparing the divided voltage Vd output from the voltage dividing circuit 74 to the reference voltage Vr1 output from the Vr1 generator 75, and outputs a binary signal in response to the comparison result. The undershoot preventive circuit 62 further includes a current control circuit 83. The current control circuit 83 controls the operation of the N-MOS transistor 81 in accordance with the signal output from the operational amplifier 82 so as to control the current ia flowing from the output terminal of the smoothing circuit 32. The operational amplifier 82, the voltage dividing circuit 74, and the Vr1 generator 75 together form a voltage determination circuit.

[00081] In the undershoot preventive circuit 62, when the mode is changed from the normal operation mode to the sleep mode, the sleep signal SLP in a high state is output from the CPU 11. Accordingly, the operational amplifier 82 and the current control circuit 83 are caused to stop the respective operations and, at the same time, the gate of the N-MOS transistor 81 is turned off and is out of conduction. Since the P-MOS transistor 41 is in an on state and is of conduction, the voltage Vo is held at a level around the power source voltage VDD.

[00082] When the mode is changed from the sleep mode to the normal operation mode, the operational amplifier 82 and the current control circuit 83 are turned into an active state and start the respective operations. At this time, the voltage Vo has a voltage close to the power source voltage VDD which is greater than the predetermined voltage Va and therefore the controller 333 outputs the voltage in a high state which turns off the P-MOS transistor 41. Therefore, the divided voltage Vd is greater than the reference voltage Vr1 and the operational amplifier 82 outputs a signal in a low state.

[00083] When the low signal is input from the operational amplifier 82 to the current control circuit 83, the current control circuit 83 raises a gate voltage Vg of the N-MOS transistor 81. As a result, the N-MOS transistor 81 generate the current ia in response to the gate voltage Vg input, as shown in Fig. 9. The voltage Vd is gradually reduced from the level of the power source voltage VDD to the predetermined voltage Va. During this reduction of the voltage Vd, the operational amplifier 82 changes the output from the low voltage to a high level

voltage when the divided voltage Vd is reduced to a level smaller than the reference voltage Vr1.

[00084] When the operational amplifier 82 outputs a high signal to the current control circuit 83, the current control circuit 83 controls the gate voltage Vg of the N-MOS transistor 81 in a way as shown in Fig. 10. That is, the gate voltage Vg is linearly raised during a predetermined time t1 and is continuously raised during a predetermined time t2. Further, the gate voltage Vg is held at a level of the power source voltage VDD during a predetermined time t3 and is reduced from the level of the voltage Vg to the grounding level during a predetermined time t4. During these operations, the current ia flowing through the N-MOS transistor 81 is changed in a way as shown in Fig. 9. The current during the predetermined time t3 is a saturated current. Also, during these operations, the voltage level of the gate voltage Vg is changed in a way as shown in Fig. 10. The gate voltage Vg is continuously raised in the predetermined time t2 at the same voltage raising pace as in a predetermined time t1 after the predetermined time t1, as shown in Fig. 10. This is because the duty control circuit 72 takes a certain delay time before starting the control of the operation of the P-MOS transistor 41 after the voltage level of the voltage Vo is changed to the predetermined voltage Va.

[00085] It should be noted that Fig. 10 shows a case in which the current control circuit 83 receives a high signal from the operational amplifier 82 before the gate voltage Vg is raised to a level of the power source voltage VDD after the

predetermined time t1 following the application of the gate voltage Vg to the N-MOS transistor 81. On the other hands, when the current control circuit 83 raises the gate voltage Vg to the level of the power source voltage VDD upon receiving a high signal from the operational amplifier 82, the gate voltage Vg changes in a way as shown in Fig. 11. In Fig. 11, a predetermined time t1' is equivalent to the predetermined time t1 of Fig. 10 but is relatively longer than the predetermined time t1, and the current control circuit 83 attempts to raise the gate voltage Vg during the predetermined time t2. At this time, however, the gate voltage Vg is raised to the level of the power source voltage VDD and, as a result, the gate voltage Vg is held at the level of the power source voltage VDD during the predetermined times t2 and t3.

[00086] The current control circuit 83 is previously provided with various kinds of settings associated with the gate voltage of the N-MOS transistor 81 so that the voltage regulator 3 starts its operation and the load current io flows from the smoothing circuit 32 through the voltage regulator 3 during the time the current control circuit 83 reduces the gate voltage of the N-MOS transistor 81 to the grounding level. More specifically, the above-mentioned various kinds of settings includes the voltage raising pace of the gate voltage Vg of the N-MOS transistor 81, the predetermined times t2 and t3 in which the gate voltage Vg is held at the level of the power source voltage VDD, and the pace of reducing the gate voltage Vg from the level of the power source voltage VDD to the grounding level.

[00087] The overshoot preventive circuit 63 is in an inactive state and maintains the output terminal at an open state in the normal operation mode. Accordingly, the overshoot preventive circuit 63 stops applying a gate voltage to the P-MOS transistor 41. In the sleep mode, the overshoot preventive circuit 63 is turned into an active state and detects a current output from the P-MOS transistor 41. Therefore, the overshoot preventive circuit 63 controls the gate voltage of the P-MOS transistor 41 in accordance with the result of the current detection.

[00088] During the sleep mode, the overshoot preventive circuit 63 raises the voltage Vo to the level of the power source voltage VDD by making the gate voltage of the P-MOS transistor 41 low to turn on the P-MOS transistor 41 when the detected current is smaller than a predetermined value □ (e.g., 1A). When the detected current is greater than the predetermined value □ (e.g., 1A), the overshoot preventive circuit 63 continuously raises the gate voltage of the P-MOS transistor 41 in response to the detected current so that the current supplied from the P-MOS transistor 41 is successively reduced to the level smaller than the predetermined value □ (e.g., 1A).

[00089] When the above-described operations are performed, the voltage Vo is changed in a way as shown in Fig. 12. As a result, the voltage Vo can be prevented from the undershooting during the time the mode is changed from the sleep mode to the normal operation mode and from the overshooting during the time the mode is changed from the normal operation mode to the sleep mode. In addition, the overshoot preventive circuit 63 also has a function for prevent an excessive

current flowing from the P-MOS transistor 41 in the sleep mode when a short circuit occurs in a load connected to the smoothing circuit 32. With this, the power supply apparatus 1 can prevent an excessive current output from the DC-to-DC converter 2 in the sleep mode.

[00090] As described above, in the DC-to-DC converter 302 of Fig. 7, the reference voltage Vr1 and the divided voltage Vd are compared by the operational amplifier 73 of the voltage detection circuit 71 and the duty controller 72 generates a pulse signal that has a duty cycle in response to the comparison result and applies the pulse signal to the gate of the P-MOS transistor 41. In this case, relationships among the voltage Vo, the divided voltage Vd, and the reference voltage Vr1 are as shown in Fig. 13, in which a portion enclosed with a chain line is shown in an enlarged form. Fig. 13 indicates that the DC-to-DC converter 302 prevents the voltage Vo from undershooting though the voltage Vo may still be dropped to a level slightly lower than the predetermined voltage Va since the DC-to-DC converter 302 is fell into an inactive-like state during the time the mode is changed from the sleep mode to the normal operation mode.

[00091] Fig. 14 shows a DC-to-DC converter 402 according to another preferred embodiment. The DC-to-DC converter 402 can be used as an alternative to the DC-to-DC converter 302 of Fig. 7 and is similar to it, except for a control circuit 433. This control circuit 433 can be used in place of the control circuit 233 of the DC-to-DC converter 202, as a further alternative. In Fig. 14,

connections of the sleep signal SLP to each component inside the control circuit 433 are not shown for the sake of simplicity.

[00092] The controller 433 of Fig. 14 is similar to the controller 333 of Fig. 7, except for additional circuits of a Vr2 generator 91, a selection circuit 92, and an operational amplifier 93 to the voltage detection circuit 71 of Fig. 7. The Vr2 generator 91 generates and outputs a reference voltage Vr2. The selection circuit 92 exclusively selects one of the reference voltages Vr1 and Vr2 in accordance with a control signal and inputs the selected reference voltage to the operational amplifier 73. The operational amplifier 93 controls the operation of the selection circuit 92 in accordance with the divided voltage Vd. Accordingly, in Fig. 14, a duty control circuit 61a replaces the duty control circuit 61 of Fig. 7 and a voltage detection circuit 71a replaces the voltage detection circuit 71 of Fig. 7.

[00093] As shown in Fig. 14, the controller 433 includes the duty control circuit 61a, the undershoot preventive circuit 62, and the overshoot preventive circuit 63. The duty control circuit 61a includes the voltage detection circuit 71a and the duty controller 72. The voltage detection circuit 71a detects the voltage Vo, and the duty controller 72 controls the duty cycle of a pulse signal input to the gate of the P-MOS transistor 41 in response to the voltage Vo detected by the voltage detection circuit 71a.

[00094] The voltage detection circuit 71a includes the operational amplifier 73, the voltage dividing circuit 74, the Vr1 generator 75, the Vr2 generator 91, the selection circuit 92, and the operational amplifier 93. In the sleep mode, as in the

case of the voltage detection circuit 71 of Fig. 7, the operational amplifier 73 and the Vr1 generator 75 are caused to stop the respective operations, and the voltage dividing circuit 74 dividing the voltage Vo to a voltage Vd outputs the divided voltage Vd. Also, the Vr2 generator 91, the selection circuit 92, and the operational amplifier 93 are caused to stop the respective operations.

[00095] Each part of the voltage detection circuit 71a starts to operate when the mode is changed from the sleep mode to the normal operation mode. The Vr2 generator 91 generates the reference voltage Vr2 and varies it at a predetermined pace such that the reference voltage Vr2 is reduced from a predetermined voltage Vx lower than the divided voltage Vd to the reference voltage Vr1 in a predetermined time period when the mode is changed from the sleep mode to the normal operation mode.

[00096] The operational amplifier 93 performs a comparison between the divided voltage Vd and the reference voltage Vr1, and outputs a low level control signal to the selection circuit 92 when the divided voltage Vd is determined as greater than the reference voltage Vr1. The selection circuit 92 inputs the reference voltage Vr2 to a non-inverse input terminal of the operational amplifier 73 upon receiving the low level control signal from the operational amplifier 93. On the other hands, the operational amplifier 93 outputs a high level control signal to the selection circuit 92 when the divided voltage Vd is determined as smaller than the reference voltage Vr1. The selection circuit 92 inputs the reference

voltage Vr1 to the non-inverse input terminal of the operational amplifier 73 upon receiving the high level control signal from the operational amplifier 93.

[00097] With the above-described operations, the voltage Vo, the divided voltage Vd, and the reference voltage Vr2 are varied in a way as shown in Fig. 15, in which a portion enclosed with a chain line is shown in an enlarged form. Fig. 15 indicates that the DC-to-DC converter 402 prevents the voltage Vo from undershooting, which is a problematic phenomenon that the voltage Vo is dropped to a level lower than the predetermined voltage Va at a time the DC-to-DC converter 402 bears a sudden load, since the DC-to-DC converter 402 is in an active state during the time the mode is changed from the sleep mode to the normal operation mode. The reference voltage Vr2 may be controlled to be declined so that the voltage Vo is reduced at a pace slower than the case shown in Fig. 15.

[00098] In this way, the DC-to-DC converter 402 can prevent the voltage Vo from undershooting and overshooting with the undershoot preventive circuit 62 and the overshoot preventive circuit 63, respectively. The DC-to-DC converter 402 further prevents the voltage Vo from undershooting when the mode is changed from the sleep mode to the normal operation mode by the arrangement that the duty control circuit 61a uses the reference voltage Vr2 which is generated and varied by the Vr2 generator 91 at the predetermined pace such that the reference voltage Vr2 is reduced from a predetermined voltage Vx lower than the

divided voltage Vd to the reference voltage Vr1 in the predetermined time period when the mode is changed from the sleep mode to the normal operation mode.

[00099] Numerous additional modifications and variations are possible in light of the above teachings. It is therefore to be understood that within the scope of the appended claims, the disclosure of this patent specification may be practiced otherwise than as specifically described herein.

[000100] This paten specification is based on Japanese patent applications, No. JPAP2001-038394 filed on February 15, 2001 and No. JPAP2001-189792 filed on June 22, 2001 in the Japanese Patent Office, the entire contents of which are incorporated by reference herein.